AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-13. (Canceled)

14. (Currently amended) A method for producing a MIS transistor comprising a semiconductor substrate, ~~source/drain regions~~ impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity [[on]] onto a surface of said semiconductor substrate using said second film as a mask to form [[an]] the impurity diffusion ~~region~~ regions including a part thereof extending below the first groove ~~by using said second film as a mask~~;

forming an insulator film on said impurity diffusion ~~region~~ regions and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of each of the impurity diffusion ~~region~~ regions of the semiconductor substrate is higher than a bottom surface of the second groove;

forming a gate insulator film in said second groove and controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than [[a]] the top surface of each of said impurity diffusion ~~region~~ regions; and

forming a gate electrode on the top surface of said gate insulator film.

15. (Previously presented) A method for producing a MIS transistor according to claim 14, wherein said second film is a semiconductor film, and further comprising:

forming a sacrificial film in said first groove before forming said second film in said first groove; and

removing said sacrificial film after removing said second film to form said second groove.

16. (Previously presented) A method for producing a MIS transistor according to claim 14, further comprising:

polishing a surface of said second film by using said first film as a stopper.

17. (Previously presented) A method for producing a MIS transistor according to claim 14, further comprising:

forming a protective film in said second groove before forming said gate insulator film in said second groove.

18. (Currently amended) A method for producing a MIS transistor comprising a semiconductor substrate, ~~source/drain regions~~ impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity [[on]] onto a surface of said semiconductor substrate using said second film as a mask to form [[an]] the impurity diffusion ~~region~~ regions including a part thereof extending below the first groove ~~by using said second film as a mask~~;

forming [[an]] a first insulator film on said impurity diffusion ~~region~~ regions and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of each of the impurity diffusion ~~region~~ regions of the semiconductor substrate is higher than a bottom surface of the second groove;

forming a gate insulator film in said second groove and on said first insulator film;

polishing said gate insulator film by using said insulator film as a stopper and controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of each of said impurity diffusion ~~region~~ regions; and

forming a gate electrode on the top surface of said gate insulator film.

19. (Previously presented) A method for producing a MIS transistor according to claim 18, wherein said second film is a semiconductor film, and further comprising:

forming a sacrificial film in said first groove before forming said second film in said first groove; and

removing said sacrificial film after removing said second film to form said second groove.

20. (Previously presented) A method for producing a MIS transistor according to claim 18, further comprising:

polishing a surface of said second film by using said first film as a stopper.

21. (Previously presented) A method for producing a MIS transistor according to claim 18, further comprising:

forming a protective film in said second groove before forming said gate insulator film in said second groove.

22. (Currently amended) A method for producing a MIS transistor comprising a semiconductor substrate, ~~source/drain regions~~ impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

diffusing an impurity [[on]] onto a surface of said semiconductor substrate by using said first film as a mask to form [[an]] the impurity diffusion ~~region~~ regions, including an elevated impurity diffusion region elevated above the channel region ~~in a groove from a channel region by using said first film as a mask~~;

forming an insulator film on said impurity diffusion ~~region~~ regions so that a top surface of each of the impurity diffusion ~~region~~ regions of the semiconductor substrate is higher than an upper level of the channel region;

removing said first film so as to form a groove on the semiconductor substrate;

forming a gate insulator film in said groove on the semiconductor substrate and controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of each of said impurity diffusion ~~region~~ regions; and

forming a gate electrode on a top surface of said gate insulator film.

23. (Currently amended) A method for producing a MIS transistor according to claim 22, further comprising:

elevating said ~~source/drain~~ elevated impurity diffusion region by an epitaxial growth technique before diffusing said impurity [[on]] onto said surface of said semiconductor substrate ~~to form said grooved impurity diffusion region including said elevated impurity diffusion region from said channel region by using said first film as a mask~~.

24. (Currently Amended) A method for producing a MIS transistor according to claim [[23]] 22, further comprising:

diffusing an impurity on said surface of said semiconductor substrate before elevating said ~~source/drain~~ elevated impurity diffusion region by ~~the~~ an epitaxial growth technique.

25. (Previously presented) A method for producing a MIS transistor according to claim 22, wherein said first film is semiconductor film and further comprising:

forming a sacrificial film on a surface of said first film; and

removing said sacrificial film.

26. (Previously presented) A method for producing a MIS transistor according to claim 22, further comprising:

forming a protective film in said groove before forming said gate insulator film in said groove.

27. (Currently amended) A method for producing a MIS transistor comprising a semiconductor substrate, ~~source/drain regions~~ impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

~~forming a high dielectric film to be a gate insulator film on said semiconductor substrate;~~

sequentially depositing on the semiconductor substrate a ~~laminated film on said~~ high dielectric film ~~by a~~ to serve as a gate insulator film and a polycrystalline semiconductor film to [[be]] serve as a gate electrode, to form a laminate structure;

etching said ~~laminated film~~ laminate structure so as to form said gate electrode and thereafter forming side walls ~~at a side~~ on sides of said gate electrode;

etching said high dielectric film so as to form said gate insulator film by using said gate electrode and side walls as a mask and forming a side wall insulator film at a side of said gate insulator film; and

diffusing an impurity [[on]] onto a surface of said semiconductor substrate to form [[an]] the impurity diffusion ~~region~~ regions including an elevated impurity diffusion region elevated from a channel region and controlling a thickness of the elevated impurity diffusion region by using said gate insulator film as a mask, so that a top surface of the gate insulator film is higher than a top surface of the elevated impurity diffusion region and that said top surface of the elevated impurity diffusion region is higher than a top surface of said channel region of the semiconductor substrate.

28. (Currently amended) A method for producing a MIS transistor according to claim 27, further comprising:

elevating said ~~source/drain~~ elevated impurity diffusion region by an epitaxial growth technique before diffusing said impurity on said surface of said semiconductor substrate ~~to form said grooved impurity diffusion region including said elevated impurity diffusion region from said channel region by using said first film as a mask~~.

29. (Currently amended) A method for producing a MIS transistor according to claim [[28]] 27, further comprising:

diffusing an impurity on said surface of said semiconductor substrate before elevating said ~~source/drain~~ elevated impurity diffusion region by the epitaxial growth technique.

30. (Canceled)

31. (Currently amended) A method for producing a MIS transistor according to claim 27, further comprising:

forming a protective film ~~in said groove~~ on the semiconductor substrate before forming said gate insulator film ~~in said groove~~ on the semiconductor substrate.

32. (Currently amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

forming a dummy film on said channel region, which borders said source/drain regions;

selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor ~~substrate~~ layers and said channel region;

diffusing an impurity [[on]] onto a surface of said semiconductor substrate to form impurity diffusion regions by using said dummy film as a mask and thereafter removing said dummy film;

depositing an insulator film on an exposed surface of said channel region to form a gate insulator film, which has a cross section of a grooved space at a center thereof; and

depositing a gate electrode on a top of said gate insulator film to form a gate electrode having a cross section of a T shape.

33-39. (Canceled)